NextGen CHIP DESIGN

NextGen

Competent & collaborative ASIC physical design experts

Combining in-depth technical expertise with good people skills to take your project through its full lifecycle.

- Providing ASIC physical design services at advanced tech nodes for 12+ years
- Taped out 50+ designs

contact@nextgen-chipdesign.com www.nextgen-chipdesign.com

Who We Are

NextGen is a UK-based specialist integrated circuit design company providing best-in-class ASIC physical design services (RTL to GDS) at cutting edge technology nodes and supporting global clients

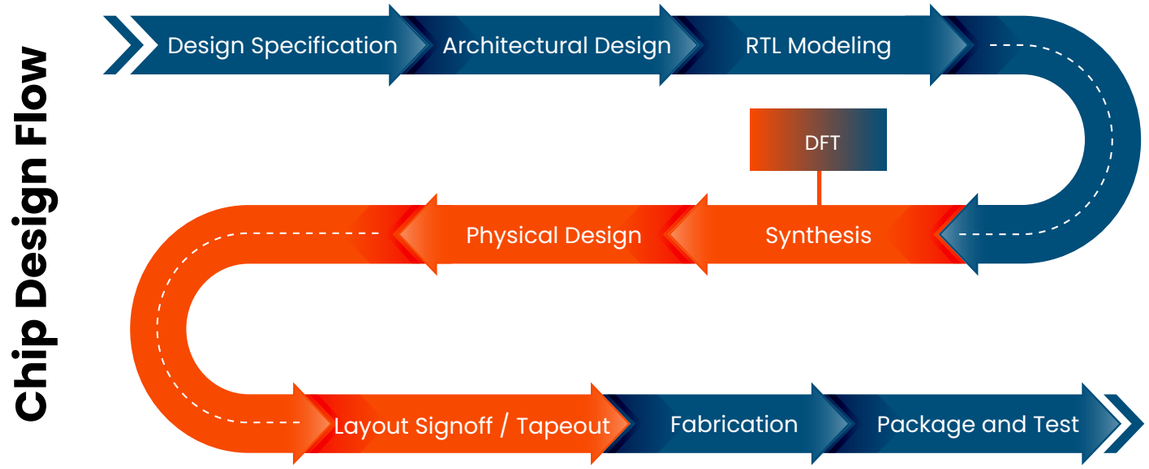
We pride ourselves on being the domain experts with extensive experience across the complete physical implementation flow(RTL to GDS) at advanced tech nodes for digital blocks, IPs, subsystems, and ASICs. Our long list of satisfied clients includes well-established semiconductor enterprises as well as the start-up ASIC design companies at the forefront of technological innovation.

NextGen has been providing ASIC physical design services for over 12 years and have taped out 50+ designs

What Do We Do

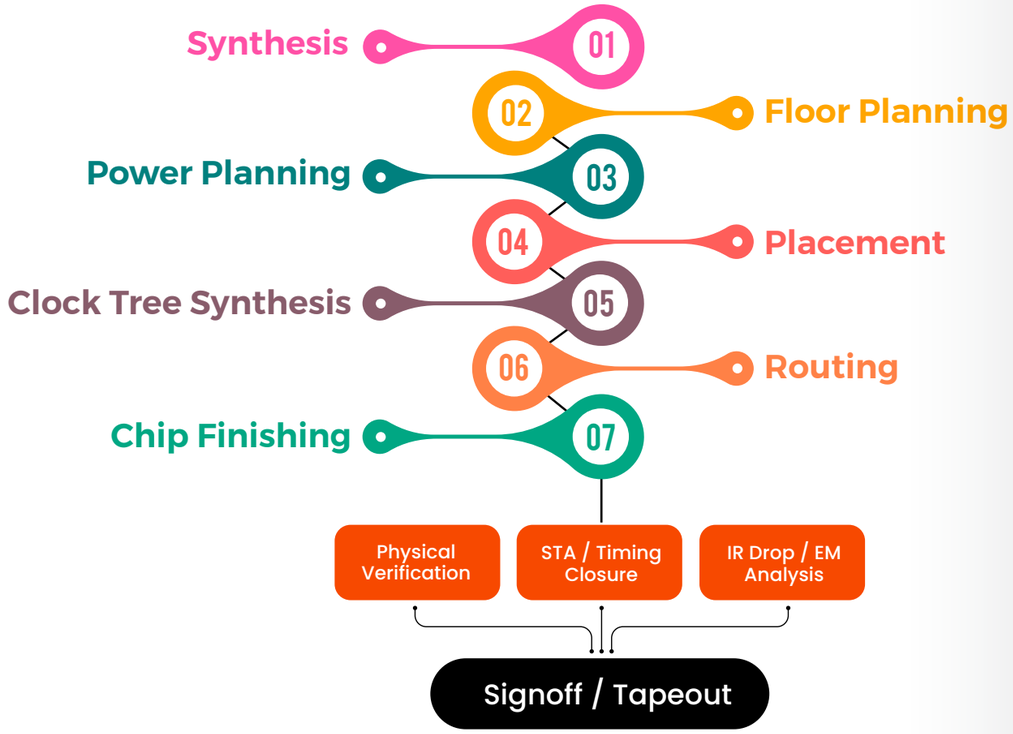
We help our clients succeed in ASIC physical design at advanced tech nodes and we believe our clients' success is our success.

We specialize in Physical design (orange highlight) from the full chip design flow.



As ASIC physical design experts, we work across the spectrum starting from RTL, doing synthesis, floor planning, power planning, place & route including clock tree synthesis, static timing analysis, physical verification, IR drop analysis and all the way to signoff & tape out.

Physical Implementation (RTL to GDS) Solutions

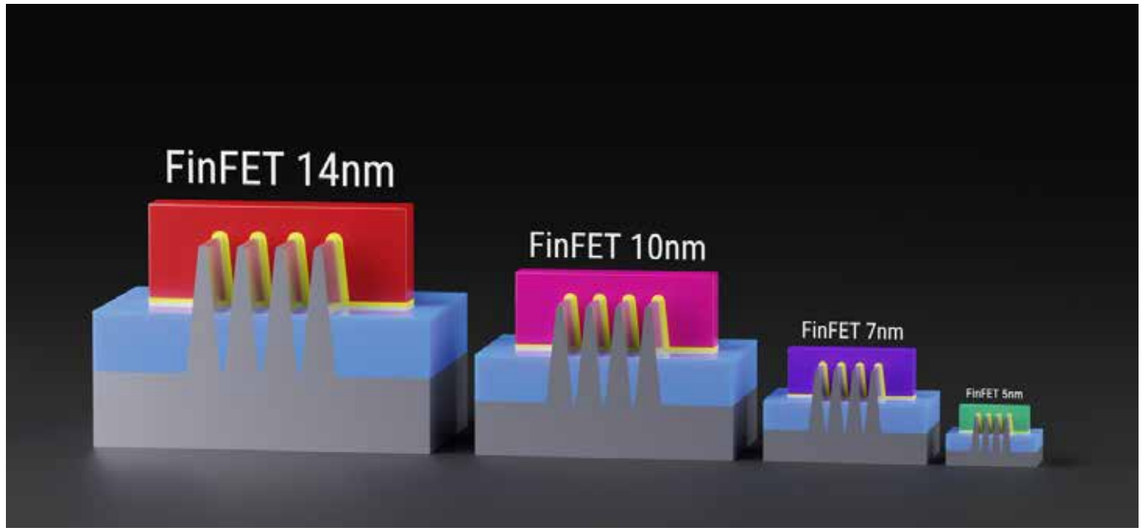


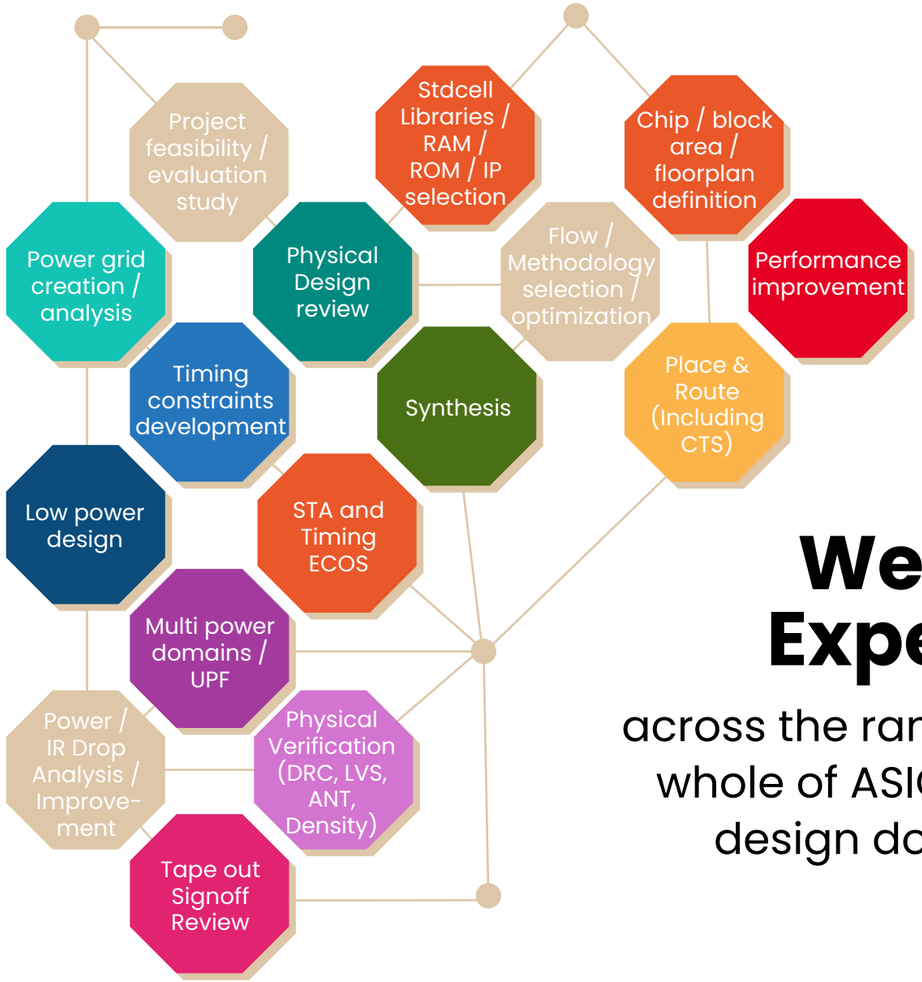
We aim to understand what our clients want to achieve and trans-form the ASIC / IP specifications and designs into working silicon bringing our clients' product ideas into reality.

Our knowledgeable, qualified and vastly experienced engineers devise the optimal and bespoke physical implementation solutions that meet our clients' specific technical specifications and business requirements.

To meet physical design objectives, we often collaborate with chip architects, RTL design engineers, IP providers, EDA vendors, DFT teams, analog teams, top-level teams, and flow & signoff teams.

We have proficiency in the EDA tools from Synopsys, Cadence and other leading EDA tools providers.



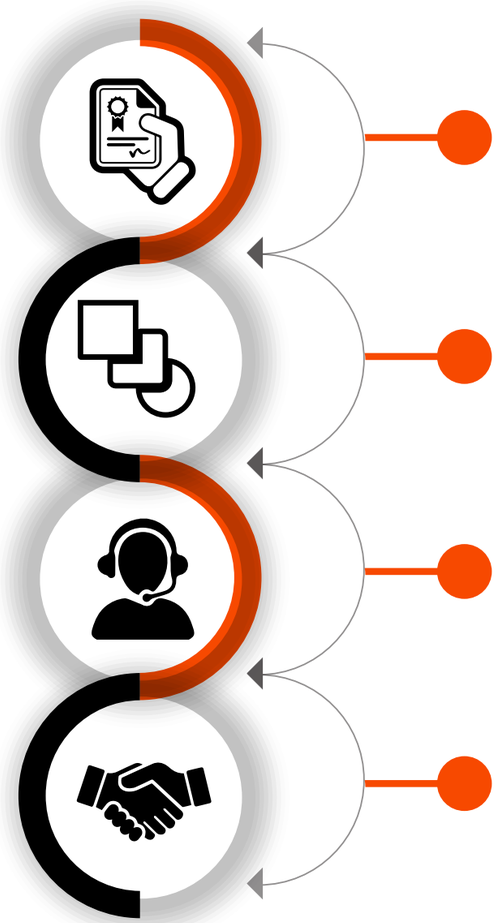


We Have Expertise

across the range for the whole of ASIC physical design domain flow

How Do We Work / Engagement Models:

We are quite flexible and can deliver bespoke solutions that meet the clients technical and business requirements. Some of the engagement models are mentioned below

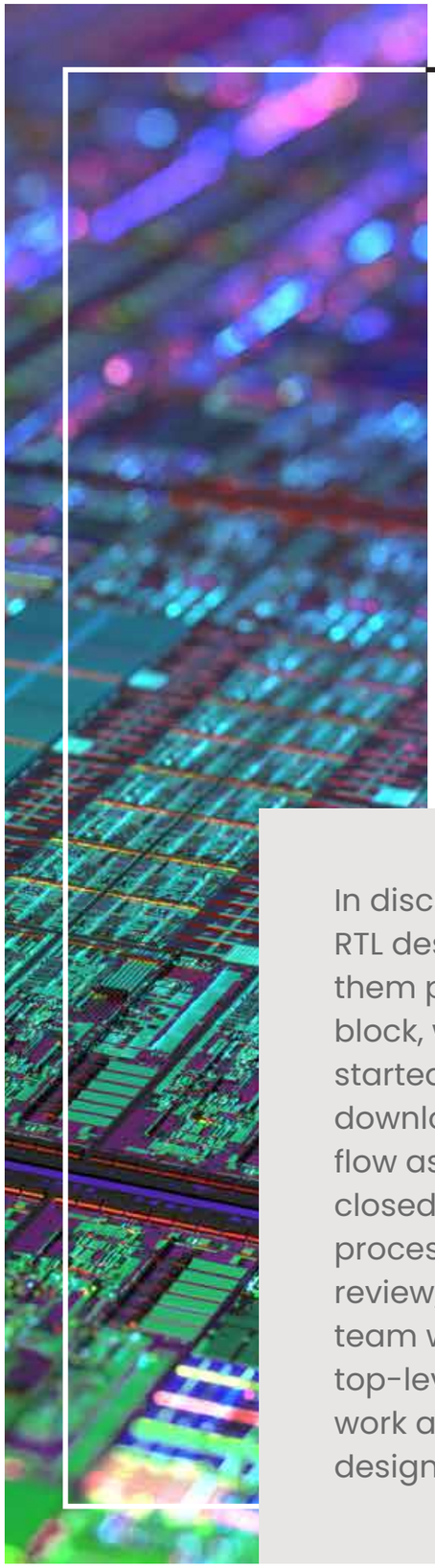


Complete ownership : We can take complete ownership of the physical design for your ASIC / IPs including the project management, starting from feasibility study, setting up the entire physical design flow from scratch, library/memory selection, synthesis, P&R, and through to tape out signoff.

Blend in : Our physical design specialists can support and blend into your existing physical design team. We can take your existing flow and do the physical design for your ASIC / IP. We can also optimize the flow as part of physical design work as appropriate.

Miscellaneous support : In case the client requires support in one specific aspect of physical design or feasibility study or physical design/signoff review or anything in between, we happily tender our expert advice to our valued clients.

Range of ASIC solutions through partnerships : Been in the semiconductors industry for a long time, we have strong connections with other functional domain experts in ASIC/IP design industry. We partner with RTL design, Functional Verification, DFT companies and domain experts to provide our clients with one-stop shop for the whole range of ASIC design solutions.



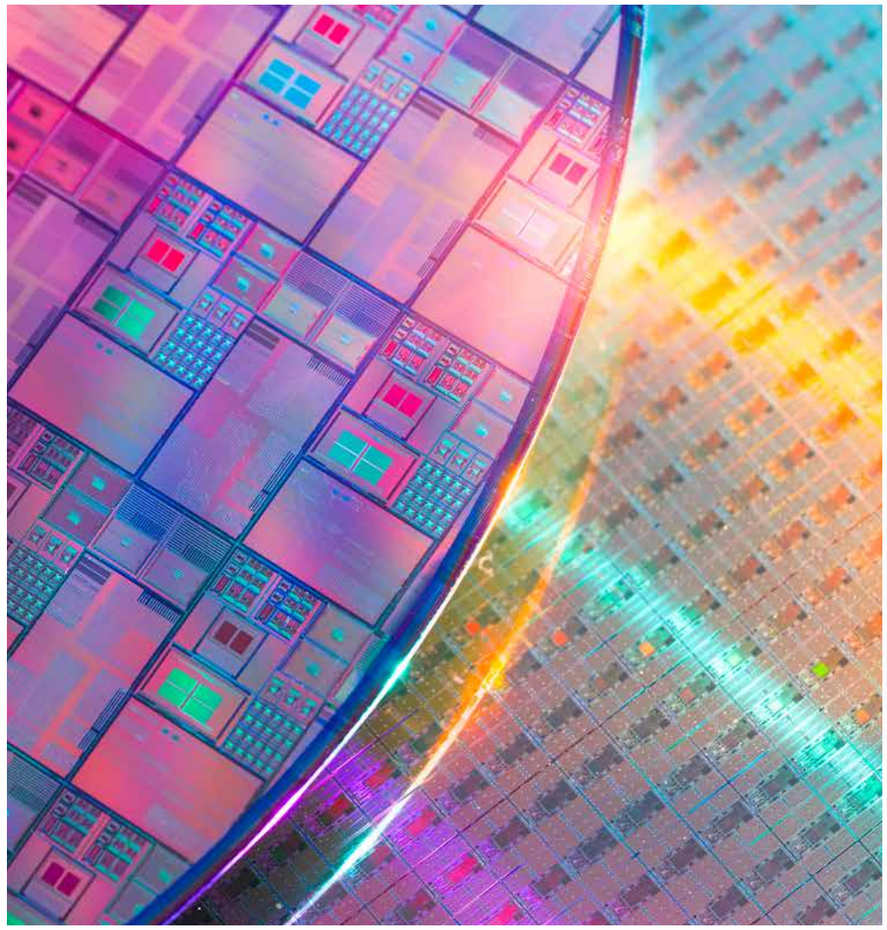
Case Study 1 :

NextGen was pleased to help one of our client, a start-up, when they needed our support for the physical design of the digital block of their first image sensor chip. The client didn't have any physical design expertise. Our starting point was the RTL of the digital block. We did all the tasks of physical design starting from synthesis, timing constraints development, P&R, STA, physical verification, and IR drop analysis.

In discussion with the top-level team and the RTL design team towards the start, we helped them provide us the floorplan of the digital block, which was an iterative process. Our team started from the physical design reference flow downloaded from EDA vendor and adapted the flow as per the design requirements as we closed the physical design following iterative process as design matured. As part of signoff review, we were pleased to help the top-level team with connectivity of the digital block at top-level too. The client was very happy with our work and they invited us to do the physical design for their next chip too.

Case Study 2:

Our client wanted help with the digital physical design of their automotive ASIC. We worked alongside their internal physical design team. We supported them with some tasks of the physical design as required like timing synthesis, timing constraints development, STA, power analysis, UPF, low power verification. The client was pleased with our help and they said they would be happy to engage us again on another project for physical design.

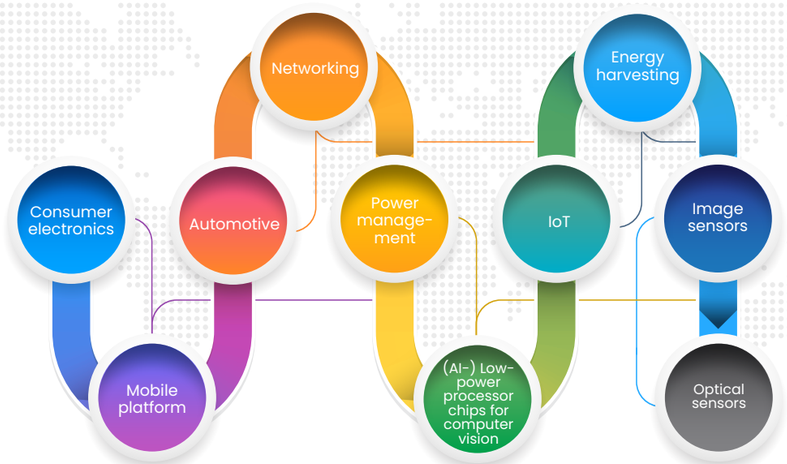


Do get in touch (by email at contact@nextgen-chipdesign.com) to discuss how we can help, and we will be pleased to help you succeed with your specific requirements.

ASIC products we have worked on

Over the years, we have successfully developed and delivered a variety of ASICs to the utmost satisfaction of our clients. We have worked with well-established semiconductor enterprises, as well as with start-up ASIC / IP design companies.

Some of the product categories that we have worked on include :



NextGen
CHIP DESIGN

NextGen

Competent & collaborative ASIC physical design experts

contact@nextgen-chipdesign.com

www.nextgen-chipdesign.com